REMARKS/ARGUMENTS

In response to the above-identified Office Action, claims 1-24 remain pending in the present application.

For the reasons set forth more fully below, Applicant respectfully submits that the present claims are allowable. Consequently, reconsideration, allowance and passage to issue of the present application are respectfully requested.

Applicant has made amendments to the specification to include serial number data of referenced U.S. Patent applications. Applicant respectfully submits that no new matter has been added by the amendments.

The Examiner rejected claims 1-24 under 35 U.S.C. 102(e) as being anticipated by Drabenstott et al ("Drabenstott"). In making the rejection, the Examiner states:

> **Drabenstott et al teaches the invention as claimed in claim 1 including a system for digital signal processing within an adaptive computing engine, the system comprising (a) a mini-matrix, the mini-matrix comprising a set of composite blocks, each composite block capable of executing a predetermined set of instructions (col. 1, line 35), (b) a sequencer for controlling the set of composite blocks and directing instruction along the set of composite blocks based on a data flow graph (col. 2, line 9; col. 5, line 48), (c) a data network for transmitting data to and from the set of composite blocks and to the sequencer (col. 6, line 43), (d) a status network for routing state word data resulting from instruction execution in the set of composite blocks (col. 2, line 15 and col. 14, line 6), and further teaches as in claims 2-9, (e) wherein each composite block is capable of executing atomic instructions, a set of n-bit instructions, asset [sic] of 16-bit instructions (conventional instructions) - claims 2, 3, and 4, (f) wherein said composite block execute [sic] multiply-alu-shift instruction on data stored in register files coupled to multiplier-alu-shifter and output result to the data network (col. 8, line 32; col. 16, line 22) - claims 3, 5, 6, (g) wherein each composite block further comprises a status register file for storing status word routed independently of data (col. 14, line 5; col. 15, line 48) - claims 7 and 8, (h) wherein the sequencer transmits instruction words subdivided into instruction field for parallel computation (col. 2, line 61; VLIW instruction contain plural sub-instructions for parallel execution in multiple units) - claim 9. The method claims 10-18 and the system claims 19-24 are equivalently rejected based on the same reason.**

Applicant respectfully disagrees with the rejection.

Drabenstott describes a single instruction multiple data stream machine with a controller and at least two processing elements to support conditional execution in a VLIW-based array processor with subword execution. While the Examiner points to the controller as being equivalent to Applicant's recited sequencer and points to the processing elements as being equivalent to Applicant's recited composite blocks, Applicant respectfully disagrees.

The present invention provides an effective combination of hardware resources in a manner that achieves multi-bit digital signal processing capability for an embedded system environment, particularly in an implementation of an adaptive computing engine. For example, independent claim 1 recites a mini-matrix, the mini-matrix comprising a set of composite blocks, each composite block capable of executing a predetermined set of instructions, a sequencer for controlling the set of composite blocks and directing instruction along the set of composite blocks based on a data flow graph, a data network for transmitting data to and from the set of composite blocks and to the sequencer, and a status network for routing state word data resulting from instruction execution in the set of composite blocks.

With the present invention, a mini-matrix is provided as a designation of composite blocks that together achieve instruction execution for multi-bit digital signal processing in an adaptive computing engine. The ability to produce effective and efficient instruction execution via the mini-matrix is supported by innovative aspects of instruction sequencing and execution. More particularly, as recited, the sequencer controlling the set of composite blocks directs instructions among the set of composite blocks based on a dataflow graph. As described in the specification on page 5, line 20+, a dataflow graph demonstrates a style of code segment representation, as shown in Figure 3, that views data as flowing from one source of computation/composite block to a destination with a capability to effectively track that.

Applicant fails to see any teaching or suggestion of the recited invention in Drabenstott, including failing to see any teaching or suggestion of a sequencer directing instructions among a set of composite blocks based on a dataflow graph. The cited lines of Drabenstott pointed to by the Examiner in the rejection with regard to the recited sequencer merely name the controller as a sequence processor. Drabenstott is silent as to any form of directing instructions based on a dataflow graph by the controller sequence processoer. Accordingly, Applicant fails to see how the sequence processor in Drabenstott anticipates or remotely suggests the recited invention that includes a sequencer directing instructions among a set of composite blocks based on a dataflow graph (see independent claims 1, 10, and 19). Without further criticality of teaching, Applicant respectfully submits that independent claims 1, 10, and 19 are allowable over the cited art.

Claims 2-9, 11-18, and 20-24 depend directly or indirectly on one of the independent claims. Thus, these claims include the features of one of the independent claims while adding further features, and therefore also are respectfully submitted as being allowable over the cited art for at least those reasons stated hereinabove. In view of the foregoing, Applicant respectfully requests withdrawal of the rejection under 35 U.S.C. 102(e).

Applicant's attorney believes that this application is in condition for allowance. Should any unresolved issues remain, Examiner is invited to call Applicant's attorney at the telephone number indicated below.

Respectfully submitted,

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